REMARKS

The Examiner objected to claim 5 because informalities stating " "instruction buffer of claim 1, a number" and is missing transitional language. Appropriate correction is required." In response, Applicants have amended claim 5 to include the transitional word "wherein."

The Examiner rejected claims 1-30 under 35 U.S.C. §102(b) as being unpatentable over Favor (US Patent Number 5,819,056).

Applicants respectfully traverse the §102(b) rejections with the following arguments.

35 USC § 102

The Examiner rejected claims 1 and 16 under 35 U.S.C §102(b) stating "Favor teaches an instruction buffer comprising: a memory array (instruction cache, element 214, figure 2 and 4) partitioned into multiple identical memory sub-arrays (figure 5) arranged in sequential order from a first memory sub-array (corresponding to element 510 instructions, figure 5) to a last memory sub-array (corresponding to element 530 instructions, figure 5), each memory sub-array having multiple instruction entry positions (rows of figure 5) and adapted to store a different instruction of a set of concurrent instructions in a single instruction entry position of any one of said memory sub-arrays (multiple instructions in each row of figure 5), said set of concurrent instructions arranged in sequential order from a first instruction to a last instruction (elements 510, 520, 530, figure 5)."

Applicants have noted that FIG. 2 of Favor includes a instruction cache 214 while FIG. 4 of Favor includes the instruction cache 214 and an instruction buffer 408, which means that Favor distinguishes between an "instruction cache" and an "instruction buffer." Applicants maintain that a cache and a buffer are clearly two different entities according to Favor and operate differently as is abundantly taught by Favor throughout the specification. Applicants do not believe the instruction cache 214 of Favor can actually operate as an instruction buffer as commonly known to one of ordinary skill in the art. Applicants further note, there is no physical description of instruction buffer 408 in Favor.

Applicants contend that claims 1 and 16 are not anticipated by Favor because Favor does not teach each and every feature of claims 1 and 16.

As a first example Favor does not teach "a physical memory array partitioned into multiple physical and identical memory sub-arrays."

Applicants respectfully point out that FIG. 5 of Favor is not a physical memory layout but a logical construct of a list 500 of instructions stored in instruction cache 214. Favor in col. 33, lines 54-56 states "The instruction cache 214 stores information in the form of a list of a plurality of instruction bytes in a predetermined order." Favor then states in col. 33, lines 62 to 64 that "Referring to FIG. 5, a list 500 is shown having three instructions 510, 520 and 530 in a sequence." Further, Favor states in col. 34, lines 1-8 that "Typically the instruction byte data and pointers are stored in binary format with the number of instructions bytes in an instruction byte data group being variable. In this example, the first instruction byte data group 512 includes four instruction bytes, the second instruction byte data group 522 includes six instruction bytes and the third instruction byte data group 532 includes three instruction bytes." Therefore, Favor is not teaching in FIG. 5 "a physical memory array partitioned into multiple physical and identical memory sub-arrays" as Applicants claims 1 and 16 require.

As a second example, Favor does not teach or suggest "multiple physical instruction entry positions." Applicants respectfully point out that Favor does not teach "multiple physical instruction entry positions", but rather a single read/write dual-directional physical port. See, for example, Favor col. 4, lines 57-59 which states "The instruction cache 214 is logically dual-ported including a read port and a write port, although the cache has only a **single** physical port."

Based on the preceding arguments, Applicants respectfully maintain that claims 1 and 16 are not unpatentable over Favor and is in condition for allowance. Since claims 2-15 depend from claim 1 and claims 17-30 depend from claim 16, Applicants respectfully maintain that claims 2-15 and 17-30 are likewise in condition for allowance.

Before discussing claims 2, 3, 17 and 18, Applicants point out that elements 512, 522 and 532 are instructions and elements 514, 524 and 534 are pointers with pointer 514 indicating the start of instruction 522, pointer 524 indicating the start of instruction and pointer 534 indicating the end of all instructions and the arrows of FIG. 5 points out this relationship, not instruction wrapping.

As to claims 2, and 17, the Examiner states "Favor teaches an instruction buffer wherein: each instruction of said set of concurrent instructions is stored in a different memory sub-array and the set of concurrent instructions may wrap from said last memory sub-array to said first memory sub-array (pointer wrapping around from element 514 to element 522 of figure 5)."

Applicants point out that Favor FIG. 5 (arrows) teach only that the instructions are stored in a sequence from the first instruction to the third instruction and there is no teaching of wrapping from the third instruction to the first instruction "within a concurrent set of instructions" as Applicants claims 5 and 17 require.

As to claims 3 and 18, the Examiner stated "(in the condition of the pointer of element 534 wrapping around to element 512 the entry position would be lower at 512 than 534)."

Applicants note that the Examiner has indicated a speculative wrapping arrow from pointer 534 to instruction 512 that does not exist in FIG. 5 and is not taught by Favor. Applicants, maintain that this does not fulfill the disclosed requirement of a §102(b) rejection.

Therefore, Applicants maintain claims 2, 3, 17 and 18 are not unpatentable over Favor and are in condition for allowance.

As to claims, 4, 5, 19 and 20, the Examiner states "Favor teaches an instruction buffer wherein each memory sub-array comprises single write port and single read port memory cells (read port and a write port, column 4, lines 49 – 59)."

Applicants point out that Favor col. 4, lines 49-59 teaches the entire instruction cache 214 has one write port and one read port, not each sub-array of the instruction cache.

Therefore, Applicants maintain claims 4, 5, 19 and 20 are not unpatentable over Favor and are in condition for allowance.

As to claims, 6 and 21, the Examiner states "for a logical entry position in the predecoder and a physical in the cache, column 4, lines 60 – 67, column 5, lines 1 – 11), each logical instruction entry position in a particular memory sub-array is a fixed number higher than an immediately previous logical instruction entry position in said particular memory sub-array (figure 7, predecoder); said physical instruction entry positions in each memory sub-array are one logical instruction entry position higher than corresponding physical entry positions of a immediately previous memory sub-array (first instruction element 710 and second instruction element 710 of figure 7), the first physical instruction entry position and first logical instruction entry position of a first memory sub-array being the same (opcode and memory location same, column 35, lines 1 -11); and each said instruction of said set of concurrent instructions is stored in consecutive logical instruction entry positions of said memory array (located on subsequent pages, column 35, lines 12 – 37)."

Applicants point out while col. 4, lines 60-67 describe instruction cache 214, Favor's col. 35 lines 1-11 and FIG. 7 describe the memory section of precoder 270 and not of instruction cache 214. Thus the Examiners arguments as the structure of memory precoder 270 is not

relevant to a §102(b) rejection based on the teaching of Favor as to instruction cache 214. Applicants, further note that FIG. 7 does not describe physical memory but only a logical organization of the memory.

Therefore, Applicants maintain claims 6 and 21 are not unpatentable over Favor and are in condition for allowance.

As to claims 7 and 22, the Examiner states "Favor teaches an instruction buffer further including: a rotator multiplexer (byte rotator, elements 430, 432, 434, figure 4) adapted to receive said set of concurrent instructions and direct each instruction of said set of concurrent instructions to an entry position (via instruction buffer, element 408, figure 4) in different consecutive memory sub-arrays (via elements 450, 452, 454, figure 4); an output multiplexer adapted to order a sequence of instructions read out of said memory array to match the order of instructions in said set of concurrent instructions (multiplexing by rotators, column 13, lines 12 – 19); a write address decoder adapted to determine a write address of a wordline (32- bit words, figure 7) of said memory array to which said first instruction of said set of instructions will be written; and a read address decoder adapted to determine a read address of a wordline (32-bit words, figure 7) of said memory array from which a first instruction of a group of instructions will be read from (read/write decoders, elements 410, 412, 414, 416, 418, figure 4, operating in decoding cycle, column 13, lines 36 – 53) .

In response, Applicants point out:

(1) Elements 450, 452 and 454 of Favor Fig. 4 are registers in macroinstruction decoder 230 not sub-arrays of instruction cache 214 thus are not relevant to a §102(b) rejection based on the teaching of Favor as to memory-sub-arrays of instruction cache 214.

(2) In Favor FIG. 4, the byte rotators 430, 432 and 434 are feeding registers 450, 452 and 454 not receiving information from them as the Examiner alleges.

(3) In Favor FIG. 4, elements 410, 412, 414, 416 and 418 are decoders reading the instruction buffers and writing to multiplexer 444 and are not separate "write address decoder adapted to determine a write address of a wordline of said memory array to which said first instruction of said set of instructions will be written" and "read address decoder adapted to determine a read address of a wordline of said memory array from which a first instruction of a group of instructions will be read from."

(4) There are no wordlines taught by Favor.

Therefore, Applicants maintain claims 7 and 22 are not unpatentable over Favor and are in condition for allowance.

As to claims 8, 9, 23 and 24, the Examiner states "Favor teaches an instruction buffer wherein: a maximum number of instructions in said set of concurrent instructions is equal to N instructions (N instructions, figure 5); said rotator multiplexer comprises N, N:1 multiplexers, each multiplexer adapted to select one of said N instructions and couple the selected instruction to one of said memory sub-arrays (rotators based on N instructions, figure 4)."

As to claims 8 and 23, Applicants point out that the rotators 430, 432 and 434 of Favor FIG. 4 are not selecting a different instruction as the Examiner alleges, but are accepting inputs from instruction buffer 408, precode expander 440 and branch target buffer 456. The actual instructions in instruction cache 214 are passed to instruction buffer 408 by precode expander 440 so all instructions go to only byte rotator 434.

As to claims 9, and 23, the claimed elements ("N/2 multiplexers" or "2:1 multiplexers") are not aught by Favor in FIG. 4 or any where else in Favor as far as Applicants can determine.

Therefore, Applicants maintain claims 8, 9, 22 and 23are not unpatentable over Favor and are in condition for allowance.

As to claims 10, 11, 25 and 26, the Examiner states "Favor teaches an instruction buffer wherein: a number of said physical entry positions in each said memory sub-array is equal to Q; N is equal to 8 and Q is equal to 8; the first instruction in said set of concurrent instructions has a physical instruction entry position defined by a 6-bit address, a first set of 3-bits of said 6-bit address defining a physical entry position in each memory sub-array and a second set of 3-its of said 6-bit address defining a position of said sub-array in said memory array (figure 4a, address field shown by circuit diagram); and said write address decoder comprises: a write wordline decoder adapted to generate an 8-bit address of said first set of 3-bits and a 1-bit to the left shifted 8-bit address of said 8-bit address; seven 2:1 address multiplexers, an output of each address multiplexer coupled to a corresponding wordline select of seven sequential memory sub-arrays beginning with said first memory sub-array, a first input of each address multiplexer coupled to said 8-bit address, a second input of each address multiplexer coupled to said shifted 8-bit address and the select input of each address multiplexer coupled to a logic circuit (column 10, lines 11 – 25), said logic circuit coupled to said second set of 3-bits; and said 8-bit address coupled to a wordline select of said last memory sub-array (buffer in each group 0-7, column 10, lines 26 – 39).

Applicants point out that there is no FIG. 4A in Favor and col. 10 lines 11-25 and 26-29 do not teach "a write wordline decoder adapted to generate an 8-bit address of said first set of 3-

bits and a 1-bit to the left shifted 8-it address of said 8-bit address; seven 2:1 address multiplexers, an output of each address multiplexer coupled to a corresponding wordline select of seven sequential memory sub-arrays beginning with said first memory sub-array, a first input of each address multiplexer coupled to said 8-bit address, a second input of each address multiplexer coupled to said shifted 8-bit address and the select input of each address multiplexer coupled to a logic circuit..., said logic circuit coupled to said second set of 3-bits; and said 8-bit address coupled to a wordline select of said last memory sub-array (buffer in each group 0-7)" as the Examiner alleges.

Further, all the Examiners arguments address the format of addresses and not the "N, N:1 multiplexers" of Applicants claims 8 and 23 or the "N, (N/2):1 first multiplexers" or the "N, 2:1 second multiplexers" of Applicants claims 9 and 24.

Therefore, Applicants maintain claims 10, 11, 23 and 24 are not unpatentable over Favor and are in condition for allowance.

As to claims 12, 13, 27 and 28, the Examiners states "Favor teaches an instruction buffer wherein: M equals 5 and a maximum number of instructions to be read out of said memory array concurrently is M instructions; and said output multiplexer comprises M, N:1 multiplexers (multiplex access to plurality of outputs, column 5, lines 66 – 67, column 6, liens 1 – 11)

Applicants point out that Favor does not teach, as the Examiner alleges, in col. 5, lines 66-67 and col. 6, lines 1-11 "wherein: M equals 5" as required by Applicants claims 12 and 26 or "a maximum number of instructions to be read out of said memory array concurrently is M instructions; and said output multiplexer comprises M, N:1 multiplexers" as Applicants claims

13 and 28 require. In fact, Favor consistently teaches that instruction cache 214 contains only three instructions.

Therefore, Applicants maintain claims 12, 13, 27 and 28 are not unpatentable over Favor and are in condition for allowance.

As to claims 15 and 30, the Examiner states ", Favor teaches an instruction buffer wherein each memory sub-array is selected from the group consisting of static random access memory arrays (SRAM, column 3, lines 64 — 67), dynamic random access memory arrays (DRAM, column 1, lines 13 — 15), latch arrays (column 5, lines 3 — 4), or a register array (1_D array, column 4, lines 4 — 6)."

Applicants have examined Favor col. 3 lines 64-67 and find no mention of an SRAM, col. 1, lines 13-15 and find no mention of a DRAM, col. 5, lines 3-4 and find no mention of latch arrays, and col. 4, lines 4-6 and find no mention of a register array as the Examiner indicates. In fact, Applicants have electronically searched Favor -and not found the terms "SRAM, DRAM, latch array or register array" anywhere in Favor."

Therefore, Applicants maintain claims 15 and 30 are not unpatentable over Favor and are in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR: Buti et al.

Dated: 09/22/2006

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